I Claim:

1. A memory cell configuration, comprising:

a semiconductor material having active regions;

word lines and bit lines;

memory cells each having a trench capacitor and a selection transistor;

said trench capacitor:

being at least partly introduced into said semiconductor material; and

being electrically conductively connected to a bit line through said selection transistor;

each of said selection transistors of said memory cells having:

a control terminal formed by a word line;

first and second terminal regions formed in an active region of said semiconductor material, said first

terminal region being conductively connected to a respective one of said trench capacitors;

said trench capacitors of said memory cells being disposed in rows;

said active regions being disposed respectively between two of said trench capacitors of said memory cells;

a connecting line electrically conductively connecting two second terminal regions of two of said selection transistors of adjacent ones of said rows to one another and forming a common terminal region for two of said trench capacitors of different rows; and

a contact bit terminal:

being electrically conductively connected to said common terminal region; and

being electrically conductively connected to a bit line.

2. The memory cell configuration according to claim 1, wherein said connecting line is introduced into said semiconductor material in the form of a doped region.

3. The memory cell configuration according to claim 1, wherein said connecting line is applied to said semiconductor material in the form of a conductive layer.

4. The memory cell configuration according to claim 3, wherein said conductive layer has a height of between approximately 10 nm and approximately 50 nm.

5. The memory cell configuration according to claim 1, wherein:

said contact bit terminal is disposed between two nearest ones of said word lines;

a further word line is disposed beside each nearest word line;

further word lines form said control terminals of said selection transistors; and

said second terminal regions are part of said common terminal region electrically conductively connected to said contact bit terminal.

6. The memory cell configuration according to claim 1, wherein:

said trench capacitor has an upwardly tapering form in cross-section;

said second terminal region of a respective selection transistor of an adjacent one of said trench capacitors is at least partly disposed above said trench capacitor; and

said contact bit terminal is at least partly disposed above said trench capacitor and is electrically conductively connected to said second terminal region and to said bit line.

7. The memory cell configuration according to claim 1, wherein said word lines are at least partly routed above said trench capacitors.

8. The memory cell configuration according to claim 1, wherein a trench capacitor has a center and is surrounded by four trench capacitors each having centers at the same distance from said center of said trench capacitor.

9. The memory cell configuration according to claim 1, further comprising amplifier circuits, said bit lines being true and complementary bit lines alternately disposed one beside the other, a true and a complementary bit line forming a bit line pair, said bit line pair being routed to one of

said amplifier circuits, said bit lines of said bit line pair being disposed in transposed fashion.

10. The memory cell configuration according to claim 1, wherein said trench capacitors of two of said rows disposed one beside the other are disposed offset with respect to one another.

11. The memory cell configuration according to claim 1, wherein:

said contact bit terminal is disposed between two rows of said trench capacitors; and

said bit lines are disposed between said rows of said trench capacitors and parallel to said rows of trench capacitors.

12. The memory cell configuration according to claim 9, wherein:

said contact bit terminal is disposed between two rows of said trench capacitors; and

at least one of said bit lines and said true and complementary bit lines are disposed between said rows of said trench capacitors and parallel to said rows of trench capacitors.

13. The memory cell configuration according to claim 1, wherein said connecting line is a doped region in said semiconductor material.

14. The memory cell configuration according to claim 1, wherein said connecting line is a conductive layer applied to said semiconductor material.

15. The memory cell configuration according to claim 1, wherein:

said contact bit terminal is disposed between two nearest ones of said word lines;

further word lines are disposed respectively beside each nearest word line;

said further word lines form said control terminals of said selection transistors; and

said second terminal regions are part of said common terminal region.

16. The memory cell configuration according to claim 1, wherein:

said bit lines are true and complementary bit lines alternately disposed one beside the other;

respective ones of said true bit line and said complementary bit line form bit line pairs;

amplifier circuits are provided;

each of said bit line pairs is routed to one of said amplifier circuits; and

said bit lines of each of said bit line pairs are disposed in transposed fashion.